LARK RF TECHNOLOGY
a Benchmark® company

Why RF and High Speed Circuits Belong Together Under One Roof in Benchmark's RF and High Speed Design Center of Innovation: How Our Capabilities in Miniaturization, Embedded Components, Packaging, Thermal Management and Antenna Design Help Achieve the Art of the Possible

By Daniel Everitt, Apurva Kulkarni, Mike McCulley, Marcus Shewmaker, Rani Awale, and Arkajyoti Chang

Introduction

In the past forty years RF, baseband and high-speed compute were all discrete boxes and functions on separate boards and modules. There was not the push for integration and miniaturization that we are starting to see today. There is no more room for these functions to be discrete anymore, and the different disciplines are coming together. Conventional technology no longer gets customers where they need to be on their product roadmap.

The trends of the past 10 years show that the heavy lifting in electronics shifted from hardware to software. That is now going asymptotic. There is only so much more heavy lifting software can do. The semiconductor industry is not improving at a rate of Moore's Law anymore. Things are getting so small you are not getting a doubling effect. It is time for hardware designers to do some heavy lifting again, so the industry can continue to make technological progress.

Benchmark's plan is to reimagine the whole foundation of electronic circuits. If you really look at conventional circuit traces, they are good up to about 10 GHz, and then their performance starts to fall off, both in high-speed digital and RF. In order to fix this problem, we needed to be able to create very high aspect ratio traces. When we say "high aspect ratio", we mean a trace about as tall as it is wide. We have invested in technology and equipment to create these high aspect ratio circuits, plus we offer a lower loss substrate base material called liquid crystal polymer (LCP). There are a half a dozen design centers that can do high density interconnect (HDI) boards, but there is no one who does HDI while utilizing the capabilities of LCP. LCP has superior power handling ability and has roughly half the loss of a polyimide, making it a great choice for a HDI board material. Both RF and digital applications have loss issues at 40 GHz. Loss translates into burning up power for the customer, and loss generates heat. Our goal is to reduce loss to improve thermal management.

We believe today's DFX (design for excellence) is inherently limiting to the designer. Whether you are in the RF or digital world, if you make electronics, we know you have SWaP (size, weight and power) problems. We can give you better performance and a more reliable design.

With our new multi-capacity RF and high-speed design center located at Lark RF Technology, a Benchmark Company, we take a holistic approach to how hardware is brought together. What are the materials? What are the best pieces in each of these areas? When we bring these pieces together, how can we solve problems in new ways? Our team is in the problem-solving business – we are not tied to a specific technology. We specialize in the art of the possible - unique approaches to solving challenging hardware problems. In this paper, we introduce some of our RF and high-speed design center capabilities.

Miniaturization: Why Size Plays a Major Role in Product Design and How We Achieve It

The evolution of the electronic and computing industry has two aspects: size and computing power (speed/frequency). Seventy years ago the first computer was built occupying an area of 1800 sq. ft. and weighing over 27 tons. Today, we carry around computers with much more computing power on a daily basis in the form of cellular devices. While the decrease in size is very apparent, the other concern is speed. Overcrowding at lower frequencies has forced many industries to shift to the millimeter wave spectrum. The military, aerospace and telecommunication industries have been constantly driving toward high frequency and high speed. However, with high speed comes challenges like signal integrity, parasitics, electromagnetic interference etc. The medical industry is also shifting toward miniaturization. Smaller form factors will launch a huge improvement in the convenience of medical equipment and increase the quality of human life. Consider the example of a Ventricular Assist Device (VAD) used by patients with a frail heart that need aid in heart-related activities. Today's VAD is a bulky device, and miniaturizing it in terms of SWaP could enable a person to carry a VAD the size of a cellular phone. The impact of SWaP design improvements in electronics will be immense. In this competitive era, if a product is to achieve market success, it is essential for it to be small, lightweight and power efficient.

To successfully resolve these challenges, Lark RF Technology uses a high-density printed circuit board substrate material known as liquid crystal polymer (LCP), which was historically used in the flexible circuit industry as an alternative to polyimide. The properties of LCP are highly suitable for high-speed circuit fabrication. It is a low loss substrate, with a dielectric that is constant at high temperatures. This ensures signal integrity at high frequencies and provides tight impedance control. Due to low loss it can also act as a solder mask. This is beneficial at higher frequencies, as solder mask is a lossy material. LCP is also hydrophobic in nature, which makes it ideal for packaging and hermetically sealing electronic components.

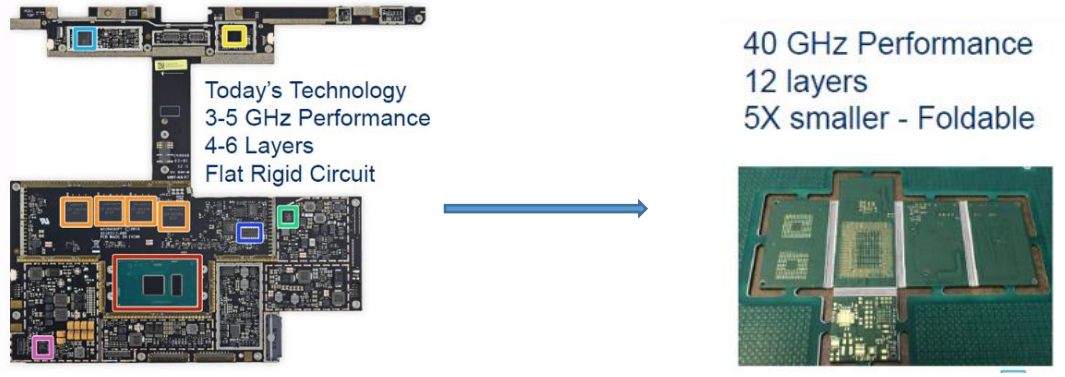


Figure 1 – Miniaturization of a Printed Circuit Board using LCP

A unique fabrication process is developed using LCP wherein the lines and spaces have the ability to be as low as 1 mil. Being able to build smaller lines and spaces with tuned performance implies we can have more circuits in a smaller area. Miniaturization of an existing board is also achieved by placing the component pads on the top layer and shifting all the traces to the layer below, while utilizing vias in the pads. Interconnects such as bus connections used to connect multiple boards in a system are components, which take up a lot of area and also add to the weight. This issue can be solved by designing embedded interconnects using LCP. LCP will also provide much needed flexibility to the interconnects, which affects the size and weight of the system. LCP's flexibility also enables the circuit to fold and fit into a miniaturized frame. Other methodologies involved in the process of miniaturization include: using passive components with smaller case sizes and utilizing bare dies. Bare dies, components and circuit lines can be buried inside LCP, thus significantly reducing the overall footprint. The innovative design guidelines allow layer count reduction by means of LCP, and thus reduce the circuit dimension in the Z direction as well.

Technology has come a long way in the last 70 years. From ENIAC, to desktops, laptops, and now by wisely using the properties of liquid crystal polymer, Lark RF Technology has shrunk computers down to an even smaller size [Figure 1 above]. With innovative design guidelines and careful utilization of unique materials like LCP, Lark RF Technology can bring about next generation miniaturization in the electronics industry, thus advancing the quality of our everyday life.

Embedded Components in Substrate for Miniaturization

A Preliminary History and Review of Comparison Materials

Liquid crystal materials were discovered by Friedrich Richard Reinitzer in the late 1880s. While experimenting with cholesteryl benzoate, he discovered the interesting properties of liquid crystals. The modern name of liquid crystals was later added by Otto Lehman. Let us fast forward to the present, where the most common printed circuit board (PCB) materials are primarily glass-filled flame resistant epoxy laminate (FR4). While FR4 is an inexpensive substrate that can handle most of the common uses it is subjected to, the ever increasing speed of modern electronics is pushing the physical and electrical

limitations of FR4 beyond its capabilities. All of the limitations are quickly adding to the need for a more resilient substrate material to replace FR4. When FR4 is placed in a moisture rich environment, it changes the high-speed characteristics of the material. Although there are many engineered coatings and hermetically sealed housings that can be added to protect the electrical characteristics of FR4 based systems, all of these items add cost and weight, and can have an impact on performance. When environmental concerns are added to the FR4 substrate equation, FR4 becomes a higher cost liability to modern circuit design. One of the newer substrate materials in the industry is polyimide. Polyimide is a high temperature, flexible substrate that can do some of the things that liquid crystal polymer can do. However, the loss tangent of polyimide keeps it in the low frequency range with FR4. The moisture uptake of polyimide is another limiting factor. All of the characteristics associated with these materials quickly paint a limiting picture as frequencies extend over 10 GHz. High speed digital circuits, thermal characteristics and the moisture absorption properties of these substrates make it difficult to predict the variables in these ever-changing systems.

Most PCBs are made with surface-mount technology (SMT) on a rigid FR4 or other costly, rigid substrates that offer performance gains. The current use of SMT puts components on the top and bottom sides of multilayer circuit boards to gain real estate in the shrinking systems. The SMT placed microchips are made from materials such as silicon, Gallium Nitride (GaN), GaS and other materials that are packaged in hermetic cases, and then wired to pads and terminals inside these cases, extending to the pads and traces on the PCBs. The added internal connections of these packages introduce additional resistance and loss. Even chip scale packages add one more layer of interconnect that can be removed from the entire system if the dies are directly attached to the connection points in embedded PCBs.

LCP as a PCB substrate exhibits excellent physical, environmental and electrical properties. The natural world produces liquid crystal (LC) materials, and has intrigued humans for centuries. The silk worm creates LC in its silk and spider webbing is a LC material. In the early 2000s people started to exploit this mesophasic state of matter with engineered versions of LCP. A primary property of LCP makes it a near hermetic solution to embed components into, due to its chemical inertness and low moisture uptake. The challenge of integrating components into the substrate of a system has been an active topic of research for many years. The culmination of all this research is reaching a boiling point, and Lark RF Technology has committed to commercializing this capability by developing a portfolio of patents focused on LCP manufacturing processes. Lark is also investing heavily in the microelectronics equipment needed to build these new designs. The embedded and integrated substrate capability is a step in the right direction to miniaturizing modern electronics. The Internet of Things (IoT) revolution set to descend on society over the next few years will influence and drive trends in modern electronics.

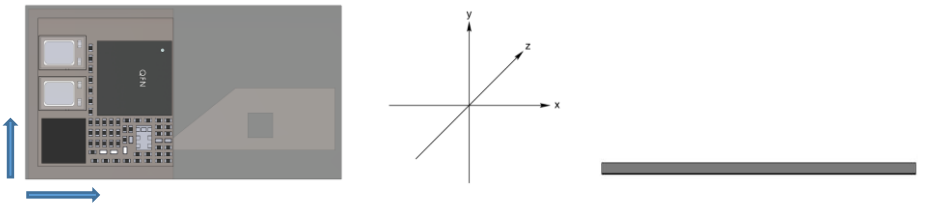
Embedding Components

Embedding components into a semi-hermetic LCP and hybrid LCP/FR4 substrate is a solution currently offered at Lark RF Technology for military, medical and commercial applications of LCP as a packaging technology. The manufacturing methods used to create systems in package (SiP) by embedding components in the substrate requires a unique balance of materials. There are many material variables that must be considered during the initial system design, including component size, type, radio frequency (RF) requirements, power usage, circuit isolation, thermal dissipation and mechanical characteristics. The layout of these microelectronic systems are heavily reliant on connecting the signals from the component attachment point by the smallest width and shortest circuit path possible. Keeping

these circuits to the smallest size helps reduce parasitic power losses and minimize isolation and radio frequency (RF) issues. Lark RF Technology's capability to create highly symmetrical 1 mil circuit lines that connect these tiny components together aids in miniaturization. In-pad vias also aid in reducing the components' overall dimensional footprint by moving the connection point to inside the component mounting pad. The number of layers needed is dependent on how many components are involved, the isolation of multiple signal paths, and the isolating ground planes that are needed for clean signals between components.

By embedding the entire component system into a packaging material such as LCP, an overall physical size reduction can be realized, especially in the Z dimension of a system package [Figure 2 below].

X, Y and Z dimensional View of Embedded components in LCP Substrate



X & Y top view **Z Dimensional View**

Figure 2 - X, Y and Z Dimensional View of Embedded Components in LCP Substrate

Choosing the correct configuration of materials helps with miniaturization and the environmental protection of the overall system. LCP offers high-speed circuit capabilities, low-loss RF transmission lines and semi-hermetic capabilities. LCP is also a chemically inert organic substrate with low moisture absorption and excellent frequency stability over a large temperature range. The copper and LCP substrate material have a closely matched coefficient of thermal expansion to alleviate delamination.

Reduce SWaP by Strategically Removing Superfluous Packaging

What is superfluous packaging? Search the internet for this term and your results will largely discuss reducing or limiting plastic overwrap or packing peanuts on consumer goods like makeup or food items. The consumer electronics industry is one of the worst offenders, where several layers of packaging allow safe delivery across the globe, such as with cellular phones. In many cases, there is a euphoric component associated with the unboxing experience. For examples of this phenomenon, search "unboxing" on YouTube. Great effort goes into making each step of the experience gratifying from the moment the package arrives to when the consumer first starts using the product.

So let us dive into the less obvious case for superfluous packaging – how we package our electronics.

Many active components used in electronics today are overmolded to aid in the robustness needed for high-speed manufacturing. Several elements are involved, including package material to protect bond

wires (this could also be hermetic lidded devices), and designing the lead frame to fan out interconnection points to more manageable pitches and lead dimensions. The package material also supplies a flat top surface to permit easy “pick and place” with automated machinery. However, this convenience to manufacturers comes at the expense of SWaP characteristics. Though packaging weight at the component level can be low, the weight and size of many SMT-ready devices are still several times heavier and larger than the die they enclose. These factors slow the race to provide ever-smaller end-use items. In terms of power, these packaged devices can reduce thermal dissipation, or at least limit the options of how thermal waste is routed from where it is generated (semiconductor die) to where it is finally eliminated from the system (chassis frame or heat sink). Such thermal restrictions compromise the system’s electrical efficiency in a feedback loop that forces elevated power requirements for a given task.

When the packaging /mold material supplied on an active device is not added to the interconnected chips within a system, this allows the chips to be brought closer in proximity before encapsulation. The result we see is the formation of SiP (system in package) architectures. This reduces SWaP, but undermines design flexibility since SiPs are typically designed and configured as COTS devices. The consumer of a SiP will almost certainly add this package to a larger system that is designed around the SiP itself – which reduces the overall design flexibility.

Optimally, a production facility would avoid this issue with control over the system design, combined with the manufacturing horsepower to actually build and validate hybrid systems. Systems would consist of custom substrates (double sided or embedded) and standard SMT components and silicon systems (stacked, flip chip and fine pitch). When design, production and validation are co-located with the functions mentioned above, design improvement iterates faster. The result is a much larger window of design flexibility while still making advances in SWaP reduction. The use of placement machinery at near-submicron accuracy will be required for upcoming substrate designs in both LCP and glass.

Another requirement for an optimal production situation would be the ability to source silicon parts in lieu of standard SMT packages. This option is available in some instances, but somewhat rare for the bulk of common silicon solutions.

An additional advantage to having hybrid designs built from beginning to end in one location is the reduction in defects due to handling and transport. “De-packaged” components are more vulnerable to die damage, disturbed bond wires, etc. Measures to encapsulate, underfill or protect components by other means can be put in place during the design process.

Thermal Management Techniques in the Miniaturization of Electronics

With the miniaturization of electronics, surface mount packages are getting smaller and smaller, leading to higher heat densities in power components. This, in turn, creates the need for a better and more optimized approach for thermal dissipation in PCBs. Applying the appropriate methods for controlling the heat dissipation will eventually allow for better functioning PCBs with higher component reliability. We will discuss the standard thermal dissipation methods used in PCBs, and then introduce some new possible approaches that create opportunities for innovative solutions in the space-constrained and high heat density environments that challenge designers in electronics today.

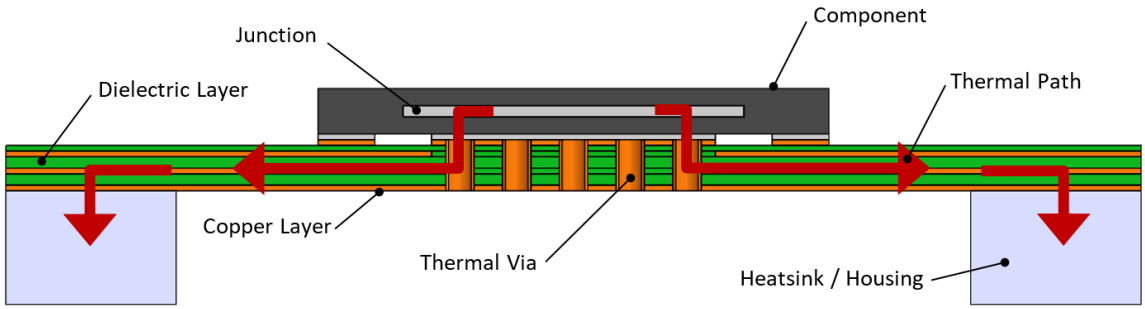


Figure 3 - Standard Thermal Dissipation Case

Figure 3 above presents a standard thermal dissipation case, with a standard power IC mounted on a PCB. The junction temperature of the component is critical to its function; so staying below the maximum allowable junction temperature is imperative. The main thermal conduction path will be from the IC bottom through the PCB, and the alternative path for thermal conduction is through the plastic case or the top of the component. The plastic packaging of most power components does not provide a good thermal path to the ambient environment. The only exception is when the power IC is designed with a thermal pad located on the top of the component. In this case, the IC is designed for a heat sink to be attached directly to the top of the IC. Then the thermal dissipation of the component through its top becomes a much more important factor in the design.

The standard approach for dissipating heat away from power components is by creating a thermal path from the power components to the layered copper planes by the use of thermal vias. A number of vias are strategically placed within the power IC footprint to provide a thermal connection to the copper layers below the IC, which in turn conduct heat away from the component. The PCB will then more efficiently dissipate the heat into the surrounding environment by connecting it to a housing or heat sink.

Optimizing the PCB Thermal Performance

- Whenever possible, strategically place power components on the board in such a way that heat is spread more evenly. The concentration of high power components in a limited area of the PCB will increase the heat density, which will lead to higher junction temperatures in the components.
- When the number of conductive layers connected to the thermal vias is increased (i.e., 4 layers vs 2 layers), the thermal dissipation efficiency of the board will improve.
- In high power designs, increasing the copper weight (i.e., from 1 oz. to 2 oz.) will increase the amount of heat that can be dissipated through the conductive layers; improving the cooling efficiency.
- When needed, a heat sink can be used on critical components to keep them within the acceptable thermal operating limits. Best practice is to place the heat sink on the most efficient thermal path to

the junction of the component; so the heat sink would not necessarily be placed on the top of the component unless the package was specifically designed to have a heat sink on top of the case.

- Maximizing the ratio of the thermal via's conductive area to the area of the power pad on the power IC will conduct heat more efficiently to the adjacent copper planes. Having a small via's conductive area thermally connected with the power pads of the package can create a bottleneck effect in the heat dissipation path of the design. The factors affecting this ratio are the number of vias used (more is usually better), the size of the via (smaller is usually better), and the plating thickness or useful conductive area of the via (thicker is usually better). Another notable factor is the depth of the via or its aspect ratio; where shorter depths have better thermal performance. Having a PCB with a thin dielectric layer would be advantageous; a good example in this case would be LCP.

In Figure 4 below, we illustrate the different kinds of thermal vias that can be manufactured as well as their thermal performance:

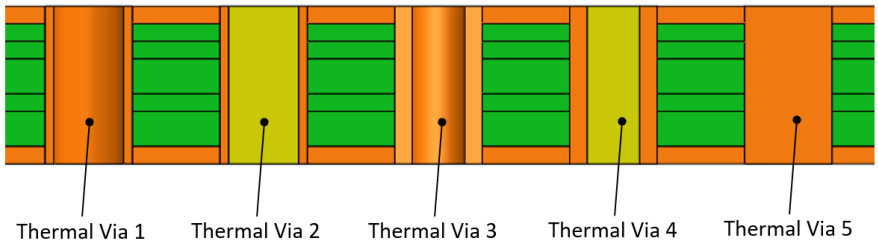


Figure 4 - Different Types of Thermal Vias

- Thermal Via 1: standard via with standard plating thickness, low thermal performance.
- Thermal Via 2: standard plating with thermal epoxy filling, improved thermal performance.
- Thermal Via 3: thicker plating on via increases thermal dissipation path for a better thermal performance.
- Thermal Via 4: thicker plating with thermal epoxy filling for an even better thermal performance.
- Thermal Via 5: copper filled via maximizes the thermal dissipation path, best thermal performance.

Optimizing Heat Dissipation in Miniature Electronics

As electronic devices shrink, the heat density of components on PCBs increases and the space available for heat management becomes significantly constrained; a good example would be mobile devices. One of the main obstacles for cooling boards would be to transfer heat from the PCB to the designated heat sink, which is not located in the vicinity of the board. Another notable challenge would be to spread the heat from a concentrated heat area to the heat sink as efficiently as possible to avoid any overheating in components. Traditionally, heat pipes or heat spreaders were used for this purpose, but even the smallest of heat pipes can have a few drawbacks in constrained assemblies. Due to these factors, specialized graphite sheets (PGS) are now becoming more important for the heat management of small electronics assemblies. In Figure 5 below we illustrate how graphite sheets can be efficiently used in constrained spaces.

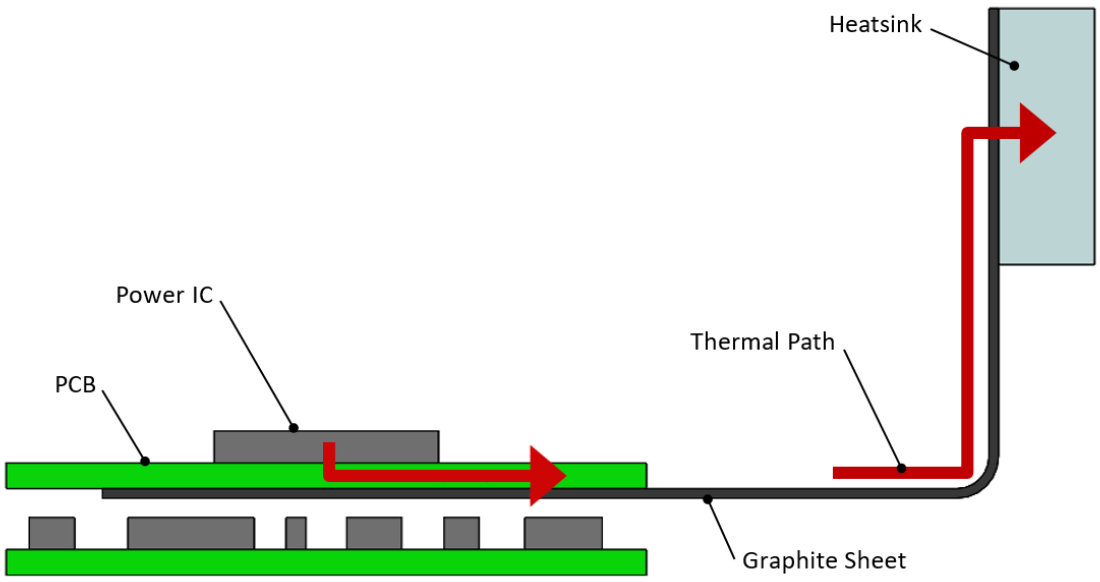


Figure 5 - Graphite Sheets

Graphite sheets (PGS) are extremely thin where typical sheets range from 10µm to 100µm in thickness, and they are very flexible, making them ideal for routing in the assembly. Most importantly, the thermal conductivity of PGS can go from 700W/mK to as high as 1950W/mK depending on the sheet thickness (figures in x/y direction). That is roughly 5X more efficient than copper in transferring heat, and it is also lighter and more cost effective. PGS can come in many different types (i.e., many thicknesses, rigid or soft for compression) which can offer multiple options when designing for heat management.

Advancement in Technology for mmWave Antennas

Introduction

With the advancement of modern manufacturing and fabrication technology, millimeter wave (mmWave) processes are becoming more commercially viable, which is leading to industry's attraction toward millimeter wave technology. Millimeter wave antenna arrays are emerging as a promising candidate in 5G systems. In addition, the high data rate of millimeter wave is becoming attractive for the technical attainment and embodiment of the Internet of Things. Due to the high data rate and small size of directive antennas at this range, radio-frequency identifiers (RFID) are also moving toward millimeter wave identifiers (MMID).

Substrate & Fabrication Challenges

Issues like path loss, rain absorption, conduction losses in metals, substrate losses and changes in substrate properties are a few well-known issues that emerge at millimeter wave frequencies. This paper focuses on the challenges of the choice of an appropriate substrate and challenges in its fabrication.

One very important variable to consider when selecting a substrate is the substrate's dissipation loss.

Though conductor losses are dominant at low frequencies, at frequencies above 10GHz, dielectric loss becomes the dominating factor contributing to the overall loss in a board. A substrate with a low loss tangent becomes very desirable at mmWave frequencies.

The water absorption in dielectric materials also becomes a driving factor in mmWave ranges. The water molecules undergo a dielectric relaxation effect at 10-100 GHz, causing the dielectric constant to drop from 80 at a few GHz to about 5, and the water also experiences a steep increase in the loss tangent. A material with a high water absorption rate increases losses in the antennas and the water absorption affects antenna gain directly. In addition, changes in dielectric constant (Dk) with frequency alter the resonant frequency of antennas at mmWave, making the antenna performance unreliable.

Stringent substrate requirements rule out several commercial substrates at mmWave. Recently, liquid crystal polymer (LCP) (Dk=3, Df=0.0016) has gained attention as a mmWave substrate solution. Characteristics like flexibility, low water absorption and low dissipation loss make LCP a promising candidate for mmWave antenna substrate. The low water absorption gives stability to LCP in a wide frequency range, which makes it a great choice of substrate for broadband antenna applications. The flexibility of LCP allows compact and conformal structures to be easier to construct and more reliable. Figure 6 below shows a conceptualization of one of these wrapping techniques, where an aperture coupled patch antenna array has its feed network on LCP wrapped on a metal block. This technique enables the placement of transceiver MMICs to be on a substrate plane perpendicular to the antenna plane. This in turn gives freedom of choosing the depth of the transceiver substrate independent from the antenna constraints for scanned arrays.

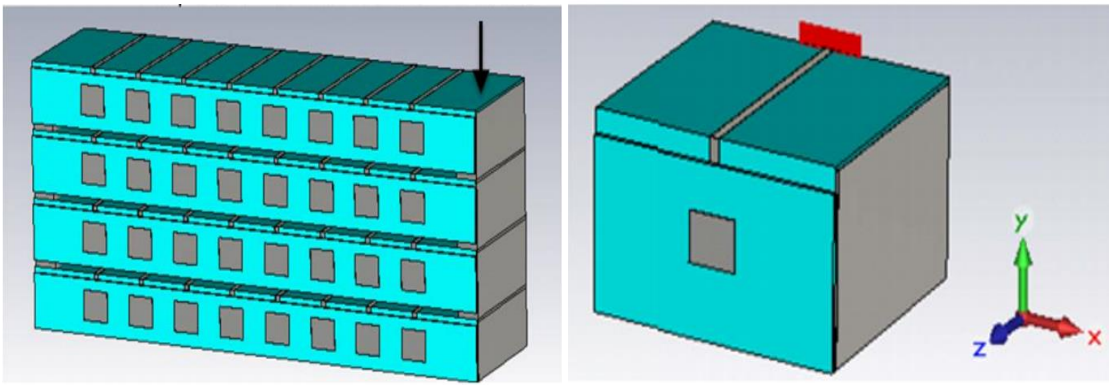


Figure 6 - Eight element array of stacked patch antenna (left), Single element of patch antenna with folded LCP substrate (right)

Fabrication precision in mmWave is a concern, since at this range of frequencies any small changes in copper traces or vias during fabrication might directly affect the conductive, as well as radiative, performance of an antenna. Signal integrity at mmWave can be ensured by utilizing the latest developments in LCP fabrication technologies.

The multilayered antenna system is a desired component in mmWave systems, as long as phased array is required. The feed network in a layer, and aperture coupling to the antenna, inherently increases performance in terms of wider band and lower cross-polarization.

Conclusion

Recent fabrication technology advances are making singular or arrays of antenna systems possible in mmWave. The advancements in precision and miniaturization are advancing the current technology toward a future horizon of high-speed systems.

Summary

Benchmark is commercializing new LCP manufacturing methods for electronic circuits at our RF and High Speed Design Center of Innovation in Phoenix under Lark RF Technology, a Benchmark Company. To our knowledge, no other company can compete with or attain our LCP manufacturing milestones. Our methods accomplish 1 mil lines and spaces in circuit traces, allowing us to support 5G and next-gen telco designs. These technical milestones enable us to set the state-of-the-art worldwide standard for LCP manufacturing. Our LCP manufacturing advances create a significant reduction in size, weight and power (SWaP) while supporting new electronics designs in military, commercial and medical markets that demand performance from 10 GHz to 100 GHz.

Our unique approach to manufacturing LCP for circuits leverages conventional processes but overcomes the historical challenges of working with LCP. LCP's multiple benefits allow next generation SWaP reduction for a wide range of electronics, IoT sensors and edge devices. Benefits include conveniently burying bare dies, components and circuit lines inside layers of a LCP printed circuit board substrate, and creating a significant reduction in the electronics-packaging footprint while maintaining a high electronic density. New LCP applications also enable unique thermal management solutions and innovative mmWave antenna designs for modern electronic applications.

References

[1] Nasiha Nikolic and Andrew Weily, "Millimeter-wave stacked patch antenna design on a folded LCP substrate," IEEE Conf. Antennas Propagat., July 2014